Applicant: MacLellean et al
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## REMARKS

In response to the Office Action mailed February 17, 2006, applicants respectfully request reconsideration. In the Office Action, claims 1-56 were rejected. By this amendment, claims 1, 6, 7, 12, 13, 17, 18, 23, 24, 29, 30, 34-36, 41, 42, 47, 48, and 52-54 have been amended and claims 55 and 56 have been canceled. Claims 1-54 remain pending in this application.

Rejections Under 35 U.S.C. §112

Claims 6, 7, 12, 13, 17, 23, 24, 29, 30, 34, 41, 47, 48, 52 and 54 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Applicant has amended the claims substantially as suggested by the examiner. Accordingly, the 35 U.S.C. §112 rejection of claims 6, 7, 12, 13, 17, 23, 24, 29, 30, 34, 41, 47, 48, 52 and 54 is moot and should be withdrawn.

Rejection Under 35 U.S.C. §102

Claims 1-56 were rejected under 35 U.S.C. §102(e) as being anticipated by Williams, U.S. Publication No. 2004/0133836. This rejection is respectfully traversed, as Williams does not teach every element recited in each of claims 1-56, as is required for a proper rejection under 35 U.S.C. §102.

Independent claim 1 recites:

A method for operating a memory system comprising:

A. receiving a digital word having N bits of data and M bits for error detection;

B. generating a first error correction code based on the N bits of data of the digital word;

C. generating a second error correction code based on the N bits of data of the digital word;

D. performing a first logic operation on the first error correction code and the second error correction code to generate a data signature representative of a comparison of the first error correction code and the second error correction code;

E. performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word;

F. comparing the generated constant signal to a predetermined constant signal to determine if an error has occurred in at least one of the N bits of data in the digital word, the M bits of data in the digital word, the first error correction code and the second error correction code; and

G. determining that an error has occurred in the N bits of data in the digital word, the M bits of data in the digital word, the first error correction code or the second error correction code if the generated constant signal is different from the predetermined constant signal.

The examiner has pointed out several components shown in Williams' Fig. 6 and has stated that each of the elements in applicants' claim1 are shown by particular components of Williams. However, an evaluation of claim 1 and the Williams disclosure shows that every element recited in claim 1 is not taught by Williams, which is required for a proper rejection under 35U.S.C. §102.

Specifically, the examiner states that Williams teaches "performing a first logic operation of the first error correction code and the second error correction code to generate a data signature representative of a comparison of the first error correction code and the second error correction code," and suggests that this is performed by Williams' component 410. Under this rationale, this would cause the output of the component 410 to be the "data signature." Next, the examiner states that Williams teaches "performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word," and suggests that this is performed by Williams' component 420.

However, while Williams' component 420 receives as an input the output of his component 410, which the examiner has equated to applicant's claimed data signature, the component 420 does not receive the M bits of the digital word, which, as recited in claim 1, are the error detection bits of the received digital word. As shown in Williams' Fig. 6, the data word (DATA IN) received comprises DATA and ECC1. The ECC1 portion of the data word DATA IN is stripped off in decoders 310A and 310B, leaving only the data portion DATA to be input to encoders 330A and 330B. See the description of decoders 310A and 310B in Paragraph 0047, lines 3-7. The ECC1 portion of the data word is not retained and not used during the remainder of the process shown in The Williams system. Therefore, the component 420 of Williams does

not and cannot perform a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word.

Furthermore, not only does component 420 of Williams not receive as inputs the data signature and the M bits of the data word, since component 420 of Williams is a 3 input OR gate, it does not and cannot generate a signal representing a comparison of the signals input thereto. If all of its inputs are zero, it will output a zero. However, any combination of ones and zeroes, or all ones, will result in an output of one. This output does not provide a comparison of the input signals.

Also, even if component 420 generated the constant signal recited in applicants' claim 1, which applicant asserts it does not, the Williams system does not compare the output of the component 420 to a predetermined constant signal, as recited in Step F of claim 1. The output of component 420 is a select signal input to multiplexer 430. It is not compared to anything.

Moreover, since Williams does not generate a constant signal and does not compare a constant signal to a predetermined constant signal, Williams does not determine that an error has occurred in at least one of the N bits of data in the digital word, the M bits of data in the digital word, the first error correction code and the second error correction code if the generated constant signal is different from the predetermined constant signal, as recited in applicants' claim 1.

Applicant notes that, in Part 53 of the Office Action, when discussing the 35 U.S.C. §103 rejection, the examiner admits that Williams does not teach every element recited in claim 1 when he states that "Williams teaches *substantially* all the limitations in claims 1-4." (Emphasis added). Section 102 requires that *every* element of a claim be taught by a reference, not substantially every element.

Accordingly, since Williams does not teach every element recited in applicants' claim 1, claim 1 is allowable over Williams and the rejection of claim 1 under 35 U.S.C. §102 should be withdrawn.

Claims 2-17 depend from independent claim 1 and are allowable for at least the same reasons as independent claim 1.

Independent claim 18 recites:

A memory system comprising:

an input portion for receiving a digital word having N bits of data and M bits for error detection;

a first error correction code generator for generating a first error correction code based on the N bits of data of the digital word;

a second error correction code generator for generating a second error correction code based on the N bits of data of the digital word;

a first logic operator for performing a first logic operation on the first error correction code and the second error correction code to generate a data signature representative of a comparison of the first error correction code and the second error correction code;

a second logic operator for performing a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word; and

a comparator for comparing the generated constant signal to a predetermined constant signal and generating an error signal indicating that an error has occurred in the N bits of data in the digital word, the M bits of data in the digital word, the first error correction code or the second error correction code.

Again, the examiner has pointed out several components shown in Williams' Fig. 6 and has stated that each of the elements in applicants' claim 18 are shown by particular components of Williams. However, an evaluation of claim 18 and the Williams disclosure shows that every element recited in claim 18 is not taught by Williams, which is required for a proper rejection under 35U.S.C. §102.

Specifically, the examiner states that Williams teaches "a first logic operator for performing a first logic operation on the first error correction code and the second error correction code to generate a data signature representative of a comparison of the first error correction code and the second error correction code," and suggests that this is performed by Williams' component 410. Under this rationale, this would cause the output of the component 410 to be the "data signature." Next, the examiner states that Williams teaches "a second logic operator for performing a second logic operation on the data signature and the M bits of the

digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word," and suggests that this is performed by Williams' component 420.

However, while Williams' component 420 receives as an input the output of his component 410, which the examiner has equated to applicant's claimed data signature, the component 420 does not receive the M bits of the digital word, which, as recited in claim 18, are the error detection bits of the received digital word. As shown in Williams' Fig. 6, the data word (DATA IN) received comprises DATA and ECC1. The ECC1 portion of the data word DATA IN is stripped off in decoders 310A and 310B, leaving only the data portion DATA to be input to encoders 330A and 330B. See the description of decoders 310A and 310B in Paragraph 0047, lines 3-7. The ECC1 portion of the data word is not retained and not used during the remainder of the process shown in the Williams system. Therefore, the component 420 of Williams does not and cannot perform a second logic operation on the data signature and the M bits of the digital word to generate a constant signal representing a comparison of the data signature and the M bits of the digital word.

Furthermore, not only does component 420 of Williams not receive as inputs the data signature and the M bits of the data word, since component 420 of Williams is a 3 input OR gate, it does not and cannot generate a signal representing a comparison of the signals input thereto. If all of its inputs are zero, it will output a zero. However, any combination of ones and zeroes, or all ones, will result in an output of one. This output does not provide a comparison of the input signals.

Also, even if component 420 generated the constant signal recited in applicants' claim 18, which applicant asserts it does not, the Williams system does not include a comparator for comparing the output of the component 420 to a predetermined constant signal, as recited in Step F of claim 18. The output of component 420 is a select signal input to multiplexer 430. It is not compared to anything. The examiner refers to comparator 410 of Williams, but it is quite clear that comparator 410 does not receive the output of component 420 as an input and does not compare the output of component 420 to a predetermined constant signal, as recited in claim 18.

Moreover, since Williams does not generate a constant signal and does not compare a constant signal to a predetermined constant signal, Williams does not determine that an error has occurred in at least one of the N bits of data in the digital word, the M bits of data in the digital

word, the first error correction code and the second error correction code if the generated constant signal is different from the predetermined constant signal, as recited in applicants' claim 18.

Accordingly, since Williams does not teach every element recited in applicants' claim 18, claim 18 is allowable over Williams and the rejection of claim 18 under 35 U.S.C. §102 should be withdrawn.

Claims 19-34 depend from independent claim 18 and are allowable for at least the same reasons as independent claim 18.

Independent claim 35 recites:

A method for operating a memory system comprising:

A. receiving a digital word having N bits of data and M bits for error detection;

B. generating a primary error correction code based on the N bits of data of the digital word;

C. generating a complementary error correction code based on the N bits of data of the digital word;

D. performing a first logic operation on the primary error correction code and the complementary error correction code to generate a data signature representative of a comparison of the primary error correction code and the complementary error correction code;

E. determining whether an error has occurred in the N bits of the digital word, the first error correction code or the second error correction code based on the value of the data signature.

Again, the examiner has pointed out several components shown in Williams' Fig. 6 and has stated that each of the elements in applicants' claim 35 are shown by particular components of Williams. However, an evaluation of claim 35 and the Williams disclosure shows that every element recited in claim 35 is not taught by Williams, which is required for a proper rejection under 35U.S.C. §102.

The examiner states that Williams teaches "performing a first logic operation on the primary error correction code and the complementary error correction code to generate a data signature representative of a comparison of the primary error correction code and the complementary error correction code," and suggests that this is performed by Williams'

component 410. Under this rationale, this would cause the output of the component 410 to be the "data signature."

However, component 410 of Williams only receives and compares the ECC signals output by each of encoders 330A and 330B. These ECC signals are generated based on the input to the decoders of the DATA portion of the DATA IN word. These ECC signals are identical if there are no errors in the DATA portion in Path A and Path B. They might be different if either DATA portion in Path A or Path B has an error. However, neither ECC code input to component 410 and compared to each other is the *complement* of the other. Nowhere in Williams is a primary error correction code compared to the complementary error correction code. Therefore, Williams does not teach or suggest "performing a first logic operation on the primary error correction code and the complementary error correction code to generate a data signature representative of a comparison of the primary error correction code and the complementary error correction code," as recited in claim 35.

Accordingly, since Williams does not teach every element recited in applicants' claim 35, claim 35 is allowable over Williams and the rejection of claim 35 under 35 U.S.C. §102 should be withdrawn.

Claims 36-54 depend from independent claim 35 and are allowable for at least the same reasons as independent claim 35.

Rejection Under 35 U.S.C. §103

Claims 12-17, 29-34 and 47-53 were rejected under 35 U.S.C. §103(a) as being unpatentable over various combinations of Williams with other cited references. This rejection is respectfully traversed.

Based on applicants' arguments above, independent claims 1, 18 and 35 are allowable over the cited references. Since claims 12-17 depend from claim 1, claims 29-34 depend from claim 18 and claims 47-53 depend from claim 35, these claims are allowable for at least the same reasons as the claims from which they depend. Accordingly, the rejection under 35 U.S.C. §103(a) is moot and should be withdrawn.

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Based on the foregoing, applicants respectfully assert that claims 1-24 are allowable over the art of record and respectfully request that a timely Notice of Allowance be issued in this application.

In the event the Patent Office deems personal contact desirable in disposition of this matter, the Office is invited to contact the undersigned attorney at (508) 293-7835.

Please charge any fees occasioned by this submission to Deposit Account No. 05-0889.

Respectfully submitted,

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